CLAIMS

What is claimed is:

1. A system comprising:

a central processing unit (CPU);

one or more cache memories, coupled to the CPU, each to store only data for loads to be processed by the CPU that have a vitality matching the latency associated with the respective cache memory;

2. The system of claim 1 wherein the one or more cache memories comprise:

a first cache memory, coupled to the CPU, to store only data for vital loads that are to be immediately processed at the CPU; and

a second cache memory, coupled to the CPU and the first cache, to store non-vital loads to be processed at the CPU.

3. The system of claim 2 wherein the one or more cache memories further comprise a third cache memory, coupled to the CPU and the second cache memory, to store data for semi-vital loads to be processed at the CPU.

4. The system of claim 3 wherein the CPU accesses to the first cache memory, the second cache memory and the third cache memory in parallel.

5. The system of claim 3 wherein vital loads are directly assigned to the first cache memory, semi-vital loads are directly assigned to the third cache memory

and non-vital loads are directly assigned to the second cache memory.

6. The system of claim 5 wherein the assignment of the loads to the respective caches is performed statically.

7. The system of claim 6 wherein the assignment of the loads is performed at a compiler.

8. The system of claim 3 wherein vital loads are to be processed at the CPU within one clock cycle.

9. The system of claim 8 wherein semi-vital loads are to be processed at the CPU within three clock cycles.

10. The system of claim 9 wherein non-vital loads are not to be processed at the CPU for at least four clock cycles.

11. The system of claim 3 wherein the first cache memory is a 265B cache and the third cache memory is a 1KB cache.

12. The system of claim 11 wherein the second cache memory is physically larger than the third cache memory.

13. The system of claim 3 wherein the first cache memory and the third cache memory operate at the same level in cache hierarchy.

14. The system of claim 3 wherein vital loads update the first cache memory and the second cache memory.

15. The system of claim 14 wherein semi-vital loads update the third cache memory and the second cache memory.

16. The system of claim 15 wherein non-vital loads update the second cache memory.

17. A method comprising:

identifying load instructions having a first vitality level by filtering out load instructions having a dependence distance greater than a predetermined clock cycle;

identifying load instructions having a second vitality level;

assigning load instructions having the first vitality level to be stored in a first cache memory; and

assigning load instructions having the second vitality level in a second cache memory.

18. The method of claim 17 further comprising:

identifying load instructions having a third vitality level after identifying load instructions having the first vitality level; and

assigning load instructions having the third vitality level to be stored in a third cache memory.

19. The method of claim 18 further comprising performing a profile, after identifying the load instructions having the first vitality level, to identify the remaining load instructions that frequently miss in the first cache memory and lines that are not used.

20. The method of claim 18 further comprising performing a profile, after identifying the load instructions having the third vitality level, to identify the remaining load instructions that frequently miss in the third cache memory and lines that are not used.

21. A computer system comprising:

a central processing unit (CPU);

a first cache memory, coupled to the CPU, to store only data for vital loads that are to be immediately processed at the CPU;

a second cache memory, coupled to the CPU, to store data for semi-vital loads to be processed at the CPU

a third cache memory, coupled to the CPU the first cache memory and the second cache memory, to store non-vital loads to be processed at the CPU;

a chipset coupled to the CPU; and

a main memory device coupled to the chipset.

22. The system of claim 21 wherein the CPU accesses to the first cache memory, the second cache memory and the third cache memory in parallel.

23. The system of claim 22 wherein vital loads are directly assigned to the first cache memory, semi-vital loads are directly assigned to the second cache memory and non-vital loads are directly assigned to the third cache memory.

24. The system of claim 23 wherein vital loads are to be processed at the CPU within one clock cycle, the semi-vital loads are to be processed at the CPU within three clock cycles and non-vital loads are not to be processed at the CPU for at least four clock cycles.

25. The system of claim 23 wherein the first cache memory and the second cache memory operate at the same level in cache hierarchy.

26. The system of claim 23 wherein vital loads update the first cache memory and the third cache memory.

27. The system of claim 26 wherein semi-vital loads update the second cache memory and the third cache memory.

28. The system of claim 27 wherein non-vital loads update the third cache memory.